REMARKS

Reconsideration of the application, in view of the above amendments and the following remarks is respectfully requested.

The examiner rejects Claim 2 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particular point out and distinctly claim the subject matter which applicant regards as the invention. The examiner states that the claim is indefinite because it is unclear at what current loop the cited error amplifier belongs. Claim 2 has been corrected accordingly.

The examiner rejects Claims 1, 3, 4, 6, 7, 10, 11, 19 and 20 under 35 U.S.C. § 102(e) as being anticipated by Tsuchiya. The examiner states that Tsuchiya shows in Figs. 1 and 2 a method of stabilizing the two current loops comprising a main current loop 30 using negative feedback for supplying current to the load and a sensing loop 10 using negative feedback for controlling current to the load. As it can clearly be seen from Figs. 1and 2, the amplifiers 10 and 30 each drive a respective output stage. The respective output stage for the amplifier 10 is a PMOS transistor 50 whereas the output stage for the amplifier 30 is an NMOS transistor 52. As it is well know to those skilled in the art, each of the transistors 50 and 52 will provide half of the output wave form depending whether the input is positive going or negative going. Therefore, each of the amplifiers 10 and 30 actively participate in supplying current to the load. Therefore, the examiner's characterization of the loop 10 as a sensing loop is clearly incorrect because it is involved in supplying half of the current to the load. Nowhere does the loop 10 control current to the load which current is provided by the main current loop 30. In fact, there is no control signal sent from the loop 10 to the loop 30. In sharp contrast, the present invention utilizes a separate sensing loop so that a separate stabilization capacitor can be used which is isolated from the stabilizing capacitor for the main current loop which is not shown or suggested by Tsuchiya. Claims 1, 6 and 14 have been amended in order to recite that the sensing loop does not supply current to the load in order to clarify this for the examiner.

The examiner rejects Claims 5, 12, 13, 14 and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Tsuchiya.

Claim 5 is dependent from Claim 1 the patentability which has been discussed above. It is therefore patentable for the same reasons. Claim 12 is dependent upon Claim 6 the patentability which has been discussed above and it is therefore patentable for the same reasons. This is also true for Claim 13. Claim 14 has been amended as discussed above to make it clear that the sensing loop does not supply current to the load and is therefore patentable over this reference. Claims 16-18 are dependent upon Claim 14 and therefore are patentable for the same reasons that Claim 14 is patentable.

The examiner has allowed Claims 9 and 15.

Accordingly, Applicants believe that the application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted by,
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